DEVICE FOR DETECTING TIMING SYNCHRONIZATION, METHOD THEREOF, AND COMMUNICATION DEVICE USING THE SAME

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a device for detecting a timing synchronization, and in particular to an improved device for detecting a timing synchronization which can precisely detect the timing synchronization in a simple structure, a method thereof, and a communication device using the same. The present application is based on Korean Patent Application No. 2001-6517, which is incorporated herein by reference.

Description of the Related Art

In general, in a digital communication device such as a digital modem, it is very important to synchronize digital data, namely a symbol in an exact timing. Accordingly, there have been suggested a variety of devices for detecting a timing synchronization.

FIG. 1 is a block diagram illustrating a conventional device for detecting a timing synchronization. As shown in FIG. 1, the device for detecting the timing synchronization includes a first power detector 101, a first semi-symbol delay unit 102, a second semi-symbol delay unit 103, a second power detector 104 and a subtracter 105.

The first power detector 101 receives a real number signal and an imaginary number signal of an input complex signal S(t), and detects a power level. The second power detector 104 receives a sample value delayed more than the input signal of the first power detector 104 by a semi-symbol period from the first semi-symbol delay unit 102 and the second semi-symbol delay unit 103, and detects a power level.

The subtracter 105 outputs a value obtained by subtracting the semi-symbol preceding power level from the second power detector 104 from the power level from the first power detector 101. Here, the output Y_k from the subtracter 105 is represented by following formula 1:

<Formula 1>

$$Y_k = (X_k X_k^* - X_{k-1/2} X_{k-1/2}^*)$$

Here, X_k represents an input signal and $X_{k-1/2}$ represents a semi-symbol period delayed signal.

The conventional device for detecting the timing synchronization outputs a greatest value at the precise sample point. Accordingly, whether the timing synchronization is performed can be discriminated according to an output level of the device for detecting the timing synchronization.

On the other hand, in order to restrict a data reception error, it is required to detect a symbol to be synchronized with a signal from a transmission side. For this, a communication device uses a timing error detector for detecting an error of a sampling timing of an input signal, and generating a signal proportional to the error, and a timing restoring circuit for restoring a timing according to the detected timing.

However, the conventional digital communication device respectively employs the device

for detecting the timing synchronization and the device for detecting the timing error, and thus has a complicated structure.

Accordingly, researches have been made to embody the device for detecting the timing synchronization by using the constitutional units of the device for detecting the timing error.

SUMMARY OF THE INVENTION

Accordingly, it is a primary object of the present invention to provide a device for detecting a timing synchronization which can easily detect the timing synchronization from a general device for detecting a timing error.

It is another object of the present invention to provide a device for detecting a timing synchronization by using a new algorithm.

The above object is accomplished by a device for detecting a timing synchronization in a communication device in accordance with the present invention, including a plurality of differential filters having a differential property transfer function, for respectively filtering a real number element and an imaginary number element from an input signal; a first power detector for detecting a power level from the real number element and the imaginary number element of the input signal that are respectively received; a second power detector for detecting a power level from the real number element signal and the imaginary number element that are respectively received from the differential filter; and a subtracter for subtracting the power level detected by the second power detector from the power level detected by the first power detector, and outputting the resultant value.

Another object is accomplished by a device for detecting a timing synchronization in a

communication device in accordance with the present invention, including a plurality of band-pass filters for respectively passing a real number element and an imaginary number element of an input signal through predetermined bands; a plurality of differential filters having a differential property transfer function, for respectively filtering the real number element and the imaginary number element of the input signal; a first power detector for detecting a power level from the real number element signal and the imaginary number element that are respectively received from the band-pass filter; a second power detector for detecting a power level from the real number element and the imaginary number element that are respectively received from the differential filter; and a subtracter for subtracting the power level detected in the second power detector from the power level detected in the first power detector, and outputting the resultant value.

Another object is also accomplished by a timing synchronization detecting apparatus in a communication device in accordance with the present invention, for outputting a timing synchronization discriminating signal, the timing synchronization discriminating signal being a difference between samples that are ahead and behind of the input signal by a predetermined symbol period.

Preferably, the timing synchronization detecting apparatus includes a timing error detecting unit for respectively semi-symbol delaying a real number element and an imaginary number element of the input signal, and subtracting the delayed signals from the real number element and the imaginary number element of the input signal; a first power detector for detecting a power level from the semi-symbol delayed signals of the input signal that are received; a second power detector for detecting a power level from the real number element and the imaginary number element that are

received from the timing error detecting unit; and a subtracter for subtracting a value, which is obtained by multiplying the power level detected by the second power detector by a predetermined coefficient, from the power level detected by the first power detector.

Further, another object is also accomplished by a method for detecting a timing synchronization in a communication device in accordance with the present invention, including a first power detecting step for detecting a power level by respectively semi-symbol delaying a real number element and an imaginary number element of an input signal; a second power detecting step for detecting a power level by delaying the real number element and the imaginary number element of the input signal respectively by one time, and then by subtracting the delayed real number element and the imaginary number element from the real number element and the imaginary number element of the input signal; a coefficient multiplying step for multiplying the power level obtained in the second power detecting step by a predetermined coefficient; and a subtracting step for subtracting the multiplied value obtained in the coefficient multiplying step from the power level obtained in the first power detecting step.

Preferably, the coefficient is 0.5.

The above object is also accomplished by a communication device in accordance with the present invention, including a timing synchronization detecting unit for outputting a timing synchronization discriminating signal, the timing synchronization discriminating signal being a difference between samples that are ahead and behind of the input signal by a semi-symbol period, respectively; a detection timing deciding unit for deciding a detection timing of the input signal according to the timing synchronization discriminating signal from the timing synchronization

detecting unit; and a data detecting unit for detecting the input signal according to the timing decided by the detection timing deciding unit.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete appreciation of the invention, and many of the attendant advantages thereof, will be readily apparent as the same becomes better understood by reference to the following detailed description when considered in conjunction with the accompanying drawings in which like reference symbols indicate the same or similar components, wherein:

FIG. 1 is a block diagram illustrating a conventional device for detecting a timing synchronization;

FIG. 2 is a block diagram illustrating a communication device in accordance with the present invention;

FIG. 3 is a block diagram illustrating a device for detecting a timing synchronization in accordance with a first embodiment of the present invention;

FIG. 4 is a graph showing output properties of the device in FIG. 3 and the device in FIG. 1 according to a timing error;

FIG. 5 is a block diagram illustrating a device for detecting a timing synchronization in accordance with a second embodiment of the present invention; and

FIG. 6 is a graph showing output properties of the device in FIG. 5 and the device in FIG. 1 according to the timing error.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

A device for detecting a timing synchronization in a communication device, a method thereof, and a communication device using the same in accordance with the present invention will now be described in detail with reference to the accompanying drawings.

FIG. 2 is a block diagram illustrating the communication device in accordance with the present invention. As illustrated in FIG. 2, the communication device 1 includes a timing synchronization detecting unit 200 or 300, a data detecting unit 2 and a detection timing deciding unit 4.

The detection timing deciding unit 4 decides a detection timing of an input signal according to a timing synchronization discriminating signal from the timing synchronization detecting unit 200 or 300. The data detecting unit 2 detects the input signal in the timing decided by the detection timing deciding unit 4.

The timing synchronization detecting unit 200 or 300 will now be explained with reference to FIGS. 3 and 5.

FIG. 3 is a block diagram illustrating the device for detecting the timing synchronization in accordance with a first embodiment of the present invention. As illustrated in FIG. 3, the device for detecting the timing synchronization 200 includes a device for detecting a frequency and timing error 10, a first power detector 203, a second power detector 206 and a subtracter 207.

The device for detecting the frequency and timing error 10 is described in detail in U.S. Patent Application No. 09/042,903 filed Oct. 5, 1999, entitled "Device for Detecting Frequency and Timing Error in Communication System", which is incorporated herein by reference. The device for

detecting the frequency and timing error 10 includes a first band-pass filter 201, a second band-pass filter 202, a third filter 204 and a fourth filter 205. Here, the first and second band-pass filters 201 and 202 serve to decrease a pattern jitter of the device for detecting the frequency and timing error 10, and thus are not essentially required.

As the third and fourth filters 204 and 205, differential property filters are used in an analog type, and semi-symbol period delay circuits or Hilbert filters are used in a digital type.

S(t) implies a baseband complex signal. A real number element of the input signal S(t) is applied to the first band-pass filter 201, and an imaginary number element thereof is applied to the second band-pass filter 202. Here, the output signals from the first and second band-pass filters 201 and 202 are X1r and X1i, and the complex signal is represented by 'X1 = X1r + jX1i'.

The first power detector 203 receives the real number signal X1r from the first band-pass filter 201 and the imaginary number signal X1i from the second band-pass filter 202, and detects a power level. In addition, the real number signal X1r and the imaginary number signal X1i from the first and second band-pass filters 201 and 202 pass through the third and fourth filters 204 and 205, and are outputted as a real number signal X2r and an imaginary number signal X2i, respectively. The complex signal is represented by 'X2 = X2r + jX2i'.

The second power detector 206 receives the real number signal X2r from the third filter 204 and the imaginary number signal X2i from the fourth filter 205, and detects a power level. The subtracter 207 subtracts the power level detected in the second power detector 206 from the power level detected in the first power detector 203.

The signal Y from the adder 207 is represented by following formula 2:

<Formula 2>

$$Y = X_1X_1^* - X_2X_2^*$$

Accordingly, the timing synchronization can be detected from a value obtained by subtracting the power level of the semi-symbol preceding signal X2 from the power level of the input signal X1.

As a result, the device for detecting the timing synchronization in accordance with the first embodiment of the present invention can be embodied by using the general device for detecting the timing error.

FIG. 4 is a graph showing output properties of the device in FIG. 3 and the device in FIG. 1 according to the timing error. As shown in FIG. 4, 64 quadrature amplitude modulation is used as a modulation method, and a roll-off factor is 0.18. A difference between an optimal point where the timing error is zero and a point where the timing error is not zero is greater in the device in FIG. 3 than the conventional device. Therefore, the device of the present invention can more easily detect and discriminate the synchronization than the conventional device.

FIG. 5 is a block diagram illustrating the device for detecting the timing synchronization in accordance with a second embodiment of the present invention. As shown in FIG. 5, the device for detecting the timing synchronization 300 includes a Gardner timing error detecting device 20, a first power detector 303, a second power detector 308, a coefficient multiplier 309 and a subtracter 310.

An example of the Gardner timing error detecting device 20 is disclosed in "Lock Detection for Timing Recovery" by G. Karam, V. Paxal and M. Noeneclaey (IEEE international conference

on communications vol 3. June 1996). In addition, the Gardner timing error detecting device 20 includes a first semi-symbol delay unit 301, a second semi-symbol delay unit 302, a third semi-symbol delay unit 304, a fourth semi-symbol delay unit 305, a first subtracter 306 and a second subtracter 307. The Gardner timing error detecting device 20 is a general synchronization detecting device.

The first power detector 303 detects a power level from a received real number element signal and an imaginary number element signal of an input signal, which are semi-symbol delayed respectively in the first and second semi-symbol delay units 301, 302.

The second power detector 308 receives a real number signal obtained by subtracting one symbol-delayed signal generated by the first and third semi-symbol delay units 301, 304 from the real number element of the input signal, and an imaginary number signal obtained by subtracting one symbol-delayed signal generated by the second and fourth semi-symbol delay units 302, 305 from the imaginary number element of the input signal, and detects a power level. The power level from the second power detector 308 is multiplied by a coefficient(0.5) in the coefficient multiplier 309. Here, a shifter may be used as the coefficient multiplier 309.

The subtracter 310 subtracts the power level outputted from the coefficient multiplier 309 from the power level detected in the first power detector 303. Then, the subtracter 310 outputs a signal Y_k represented by following formula 3:

<Formula 3>

$$Y_k = X_k X_k^* - (X_{k+1/2} - X_{k-1/2})(X_{k+1/2} - X_{k-1/2})^*$$

In formula 3, X_k is an input signal, $X_{k+1/2}$ is a semi-symbol period preceding signal, and $X_{k-1/2}$ is a semi-symbol period delayed signal.

Accordingly, the output signal from the device in FIG. 5 becomes a value obtained by subtracting a power level of a difference between the semi-symbol period preceding sample and the semi-symbol period succeeding sample from the power level of the optimal sample point, thereby detecting the timing synchronization.

FIG. 6 is a graph showing output properties of the device in FIG. 5 and the device in FIG. 1 according to the timing error. As shown in FIG. 6, quadrature phase shift keying is used as a modulation method, and a roll-off factor is 0.3.

The device in FIG. 5 has a greater value in an optimal point where the timing error is zero than the conventional device, and has a smaller value in a point where the timing error has the greatest value than the conventional devices. As a result, the device of the present invention has more excellent synchronization detection performance than the conventional device.

Although the preferred embodiments of the present invention have been described, it is understood that the present invention should not be limited to these preferred embodiments but various changes and modifications can be made by one skilled in the art within the spirit and scope of the present invention as hereinafter claimed. In this embodiment, the value obtained by subtracting the power level of the difference between the semi-symbol period preceding sample and the semi-symbol period succeeding sample from the power level of the input signal is outputted as the timing synchronization discriminating signal. However, it is also possible to calculate a power level of a difference between preceding and succeeding samples of a symbol period, instead of the semi-

symbol period.

As discussed earlier, in accordance with the present invention, the timing synchronization can be easily detected by using the general device for detecting the timing error.

Moreover, the timing synchronization can be precisely detected by using the new algorithm.